

AK9757W

IC for IR Sensor based thermometer

1. General Description

AK9757W is a non-contact infrared temperature sensor IC and is intended to be used in combination with AK9791W, which is an InfraRed(IR) sensor. There is a Built-in Temperature Sensor to measure the temperature of the AK9757W itself. Calculates the temperature in the FOV from IR sensor and Built-in Temperature Sensor outputs after AD convert. The parameter for temperature calculation are programmable and can be adjusted to suit the application. This device has an interrupt function and can be set to interrupt notification by INTN.

	Z. Features
Non-contact temperature measure	ments using Quantum InfraRed sensor (IR sensor)
Integrated Temperature sensor:	measurements of the AK9757W
AD Converter:	16-bit resolution
Integrated FOV Temperature calcu	lation circuit: Calculates the temperature in the FOV from IR sensor and Built-in Temperature Sensor outputs.
Integrated Digital Filter:	Cutoff frequency 1.12Hz (Output Data Rate 10Hz)
I ² C interface:	Standard Mode (100kHz) and Fast Mode (400kHz)
Interrupt Function:	Interrupt notification by INTN
Power Supply:	1.65 to1.95V
Low current consumption:	1μA(Typ.)@Stand-By 7μA(Typ.)@10Hz(Low power) 88μA(Typ.)@10Hz(High SNR)
Form of delivery :	Wafer
Class of Quality:	Consumer product grade
Size	8-pad / 1.1000mm x 1.1998mm
Application Examples:	Non-contact body surface temperature measurements, Attachment and removal detection of wearable devices

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4. Block Diagram and Functions

4.1. Block Diagram

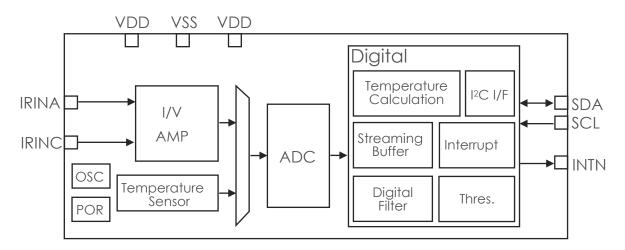


Figure 4.1. AK9757W Block Diagram

4.2. Functions

Table 4.1. Function

Table 1111 director					
Block	Function				
OSC	Built-in oscillator.				
POR	Power-On Reset circuit.				
Temperature Sensor (Temp. Sensor)	Built-in temperature sensor. Measure of the IC temperature.				
I/V AMP	I/V AMP converts the output current of the IR sensor to voltage and adjust the gain and offset of the sensor output.				
ADC	Converts the analog output of the IR sensor and the Temp. Sensor to digital signals.				
Temperature Calculation (Temp. Calc.)	From the IR sensor output and the Temp. Sensor data AK9757W can calculate the FOV temperature. The result can be read via I ² C.				
Streaming Buffer	Max. 10 data can be stored.				
Digital Filter	Digital filter (LPF) for Temp. Calc. results and the Temp. Sensor. In addition, it is possible to bypass this filter.				
Thres.	Threshold judgement Temp. Calc. results is compared with threshold levels.				
Interrupt	Interrupt function INTN goes to active when data is ready to be read, when the calculation result exceeds the threshold when the streaming buffer becomes full, or when calculation data is overflow.				
I ² C I/F	Interface to external host MCU. SCL and SDA are available for I ² C interface. Support Standard Mode (100kHz) and Fast Mode (400kHz).				

5. PAD Configurations and Functions

5.1. PAD Configurations

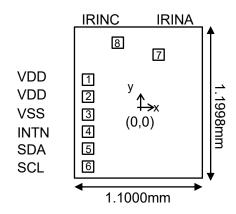


Figure 5.1. PAD Configurations

Table 5.1. PAD size and location

Chip size: 1.1000×1.1998mm Chip size includes 60µm of scribe width.

			- 1
PAD	PAD	Size(x,y)	Location(x,y)
No.	Name	[µm]	[µm]
1	VDD	80, 80	-448.24, 178.31
2	VDD	80, 80	-448.24, 70.92
3	VSS	80, 80	-448.24, -35.12
4	INTN	80, 80	-448.24, -136.53

PAD	PAD	Size(x,y)	Location(x,y)
No.	Name	[µm]	[µm]
5	SDA	80, 80	-448.24, -274.98
6	SCL	80, 80	-448.24, -446.53
7	IRINA	80, 80	165.3, 294.61
8	IRINC	80, 80	-165.3, 453.6

5.2. Functions

Table 5.2 Functions

PAD No.	PAD Name	I/O	Function
1	VDD	-	Power Supply
2	VDD	-	Power Supply
3	VSS	-	GND
4	INTN	0	Interrupt It goes to "L" in the following case. (1) when measurement data is ready to read (2) when FOV temperature data exceeds the upper or lower threshold (3) when streaming buffer is full (4) when calculation data is overflow The INTN is an open drain output (N-type transistor). This pad must be connected to a pull-up resistor.
5	SDA	I/O	I ² C Data Input/Output It is composed of a signal input and an open drain output (N-type transistor). This pad must be connected to a pull-up resistor.
6	SCL	I	I ² C Clock Input Signal processing is executed on rising and falling edge of SCL clock. This pad must be connected to a pull-up resistor.
7	IRINA		Connection pad for Anode of IR element.
8	IRINC		Connection pad for Cathode of IR element.

6. Absolute Maximum Ratings

(VSS=0V)

Parameter	Symbol	Min.	Max.	Unit
Power Supply	VDD	-0.3	2.5	V
Input Current	lin	-10	10	mA
Input Voltage	Vin	-0.3	2.5	V
Storage Temperature	Tst	-40	85	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS=0V)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power Supply	VDD	1.65	1.8	1.95	V
Operating Temperature	Ta	-30	25	85	°C

8. Power Supply Conditions

(Unless otherwise specified, VDD=1.65 to 1.95V, Ta = -30 to 85°C)

Parameter		Symbol	Min.	Тур.	Max.	Unit
Power Supply Rise Time (*1, *2)	Time until VDD is set to the operating voltage from 0.2V.	PSUP	1μ		50m	S
Power-On Reset Time (*1, *2)	Time until AK9757W becomes Stand-By Mode after PSUP.	PORT			100	μs
Shutdown Voltage (*2, *3)	Shutdown Voltage for POR re-starting.	SDV			0.2	V
Power Supply Interval Time (*1, *2, *3)	Voltage retention time below SDV for POR re-starting.	PSINT	100			μs

- *1. Reference data only, not tested in production.
- *2. Power-On Reset circuit detects rising edge of VDD, resets the internal circuit, and initializes the registers. After POR circuit works, the AK9757W is set to Stand-By Mode.
- *3. Unless this condition is satisfied, reset may not be correctly performed.

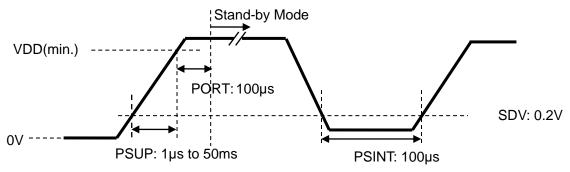


Figure 8.1. Power Supply Conditions

9. Electrical Characteristics

9.1. Total Characteristics

(Unless otherwise specified, Ta = 10 to 45°C, VDD=1.8V)

Parameter		Symbol	Min.	Тур.	Max.	Unit
IR output resolution				16		bit
Built-in Temp. Sensor	output resolution			16		bit
Temp. Calc. output re	solution			16		bit
	I/V AMP Gain : x2	SIR0		± 2.08		
I/V AMP	I/V AMP Gain : x1	SIR1	± 2.91	± 4.15		
Input Range	I/V AMP Gain : 1/2	SIR2		± 8.31		nA
iliput ixaliye	I/V AMP Gain : 1/4	SIR3		± 16.6		
	I/V AMP Gain : 1/6	SIR4		± 24.9		
IR output Noise	Ta=35 °C, ODR:10Hz I/V AMPGain:x1, AVN=1FH, LPF:off, IROFF="1"	SON			140	LSBrms
IR offset	Ta=35 °C, I/V AMP Gain : x1 IROFF="1"	SO	-145		145	LSB
Built-in Temp. sensor output code	Ta = 35 °C, OTS="0",GTS="0"	TOE	505	5041	9596	LSB
Built-in Temp. Sensor resolution (*5)	Calculated from output codes for Ta=10 °C and Ta=45 °C, GTS="0"	TSRES		1.98		mºC/ LSB
Built-in Temp. Sensor output Noise	Ta=35 °C, ODR:10Hz, AVN=1FH, LPF:off	TON		15.1	25.2	LSBrms
	Stand-By Mode	ISB		1.0	3.0	μA
Average Current Consumption	Continuous Mode ODR:10Hz AVN=00H	IDD1		7.0	10.0	μА
	Continuous Mode ODR:10Hz AVN=13H	IDD2		88.0	100.0	μА

^{*4.} Reference data only, not tested in production.

9.2. Digital Characteristics

9.2.1. DC Characteristics

(VDD=1.65 to 1.95V, Ta= -30 to 85°C, unless otherwise specified)

Parameter			Symbol	Min.	Тур.	Max.	Unit	
High level input Voltage			SCL, SDA	VIH	70%VDD			V
Low level input Voltage		SCL, SDA	VIL			30%VDD	V	
Input current	out current Vin=VSS / VDD		All pad	IIN	-10		10	μΑ
Hysteresis Input Voltage (*5)		SCL, SDA	VHS	10%VDD			٧	
Low level outputIOL= 3mAVoltageIOL= 300μA		SDA INTN	VOL			20%VDD	V	

Note:

9.2.2. AC Characteristics (1): Standard Mode (100 kHz)

(VDD=1.65 to 1.95V, Ta= -30 to 85 °C, unless otherwise specified)

Parameter		Symbol	Min.	Тур.	Max.	Unit
SCL Frequency		fSCL			100	kHz
SDA bus idle time to the next command input		tBUF	4.7			μs
Start condition Hold time		tHD:STA	4.0			μs
Clock Low period		tLOW	4.7			μs
Clock High period		tHIGH	4.0			μs
Start condition set-up time		tSU:STA	4.7			μs
Data hold time		tHD:DAT	0		3.45	μs
Data set-up time		tSU:DAT	250			ns
Rise time SDA, SCL (*6,*7)	SDA, SCL	tR			1.0	μs
Fall time SDA, SCL (*6,*7)	SDA, SCL	tF			0.3	μs
Stop condition set-up time		tSU:STO	4.0			μs

- * 6. Reference data only, not tested in production.
- * 7. CL≤400pF for SDA

^{*5 .} Reference data only, not tested in production.

9.2.3. AC Characteristics (2): Fast Mode (400 kHz)

(VDD=1.65 to 1.95V, Ta= -30 to 85 °C, unless otherwise specified)

Parameter		Symbol	Min.	Тур.	Max.	Unit
SCL frequency		fSCL			400	kHz
Noise suppression time		tSP			50	ns
SDA bus idle time to the next command input		tBUF	1.3			μs
Start condition Hold time		tHD:STA	0.6			μs
Clock Low period		tLOW	1.3			μs
Clock High period		tHIGH	0.6			μs
Start condition set-up time		tSU:STA	0.6			μs
Data hold time		tHD:DAT	0		0.9	μs
Data set-up time		tSU:DAT	100			ns
Rise time (*8,*9)	SDA, SCL	tR			0.3	μs
Fall time (*8,*9)	SDA, SCL	tF			0.3	μs
Stop condition set-up time		tSU:STO	0.6			μs

- * 8. Reference data only, not tested in production.
- * 9. CL≤400pF for SDA

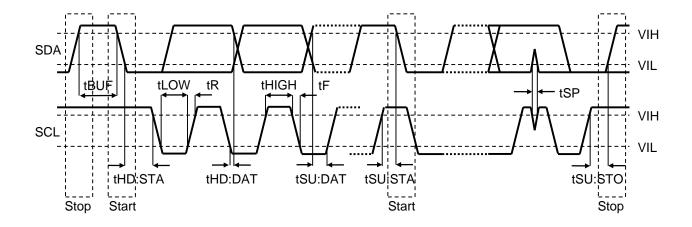


Figure 9.1. Bus Timing

9.2.4. AC Characteristics (3): INTN

(VDD=1.65 to 1.95V, Ta= -30 to 85°C, unless otherwise specified)

Parameter	Symbol	Min.	Тур.	Max.	Unit	
Rise time (* 10., * 11.)	INTN	tR			2	μs
Fall time (* 10., * 11.)	INTN	tF			0.25	μs

- * 10. Reference data only, not tested in production.
- * 11. When the load circuit of Figure 9.2 is connected.

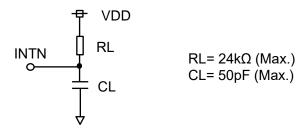


Figure 9.2. INTN Output Load Circuit

10. Functional Descriptions

10.1. System Configuration

AK9757W is intended to be used in combination with FOV Limiter, AK9791W, and Host MCU. The incident light of AK9791W is limited by the FOV Limiter.

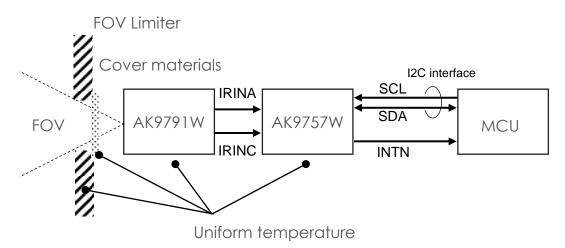


Figure 10.1.Connection Diagram

The calculation assumes that the temperatures of Field of View (FOV) Limiter, AK9791W and AK9757W are uniform. The AK9757W and a Host MCU should be connect by I²C interface (SCL and SDA). Via I²C interface, operating mode of the AK9757W is selected, and measurement data is read out. The INTN output can be used as an interrupt control signal.

Refer to Recommended External Circuits (Figure 13.1) for details.

Table 10.1. Temperature conditions

Parameter	Min.	Тур.	Max.	Unit
Recommended environmental temperature range	32		42	°C
Calculable environmental temperature range	0		50	°C
Temperature range of measurement object	32		42	°C
Measurement range of the built-in temperature sensor	-20		75	°C

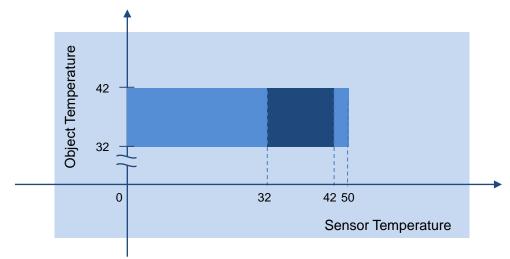


Figure 10.2. Temperature conditions

10.2. Reset function

The AK9757W is initialized in the following conditions,

10.2.1. Power-On Reset(POR)

When VDD turns on, the AK9757W is reset by the Power-On Reset (POR) circuit after VDD reaches operating voltage. After POR, the AK9757W enters Stand-By Mode and all registers are set to initial values.

10.2.2. Software Reset

The AK9757W is reset by writing Software Reset (SRST) register.

After writing "1" into SRST bit in CNTL1, the AK9757W returns acknowledgement, then the AK9757W enters Stand-By Mode and all registers are set to initial values.

10.3. Operating Mode

There are two operation modes.

10.3.1. Stand-By Mode (*MODE* = "0")

The AK9757W enters Stand-By Mode after reset (POR or Software RST) or *MODE* = "0". All circuits are powered down except for serial interface circuit. All registers can be accessed in this mode. When the AK9757W enters Stand-By Mode (*MODE* = "0"), parameters and measurement data in registers are retained, and INTN is set to the initial state ("H") in this mode.

10.3.2. Continuous Mode (*MODE* = "1")

When Continuous Mode is selected, measurement is automatically repeated at a constant rate which is selected by ODR setting. The read-out registers will be updated after measurement is completed. When *MODE* = "0" is written during a measurement, the measurement is interrupted.

Then the last measurement data which is before interruption is retained in the registers.

10.4. ODR(Output Data Rate)

Output Data Rate(ODR) is selected by ODR register.

Average Number (AVN) is selected by AVN register.

The value of Average number is limited by the *ODR* setting. There is a trade-off between the average number and the current consumption, so choose the suitable setting for your application. These registers should be written during *MODE* = "0"

10.5. I/V AMP, ADC

I/V AMP converts output current of IR sensor elements into voltage signals. Conversion gain is selected by *GAIN* register.

By setting the *IROFF* register, the input of I/V AMP can be disconnected from sensor and be shorted both inputs.

ADC has 16-bits of resolution. It converts voltage signal of I/V AMP and Built-in Temperature Sensor(Temp. Sensor) into signed 16-bit digital value.

Table 10.2. I/V AMP Gain

Table 10.2. I/ V / WII Gaill					
GAIN[2:0]	Gain				
000	x2				
001	x1				
010	x1/2				
011	x1/4				
100	x1/6				
101	Do not use				
110	Do not use				
111	Do not use				

Table 10.3. I/V AMP Input

IROFF	Input
0	IR ON
1	IR OFF
	Short-circuit the IR sensor inputs, IRINA and IRINC, inside the AK9757W.

This register should be written during *MODE* = "0"

10.6. Built-in Temperature Sensor(Temp. Sensor)

Temp. Sensor measures the temperature of the AK9757W itself. The output signal is converted to AD. Measurement range of the built-in temperature sensor is -20 to 75 °C.

10.7. correction circuit

Corrects the IR sensor output and TSENS output after AD conversion using a linear function. The correction parameters are selected by *GTS,OTS,GIT,GIR* and *OIR* registers.

$$TS' = (1 + gts) \times TS + ots$$

 $GIR' = git \times TS'$
 $IR' = (gir + gir \times GIR') \times IR + oir$

IR: IR sensor output after AD conversionTS: Temp. Sensor output after AD conversion

Table 10.4. correction parameters

65 1 1 1			· · · ·	
coefficient	Type	Register	Value	Description
orto	oignod	GTS[7:0]	gts = GTS × 2 ⁻¹⁰	TS Gain
gts	signed	G13[7.0]	-0.125 to +0.124	default : 0
ots	signed	OTS[13:0]	ots = OTS	TS Offset
บเร	ots signed	013[13.0]	-8192 to +8191	default : 0
			git = GIT × 2 ⁻²³	Temperature dependent
git	signed	GIT[7:0]	-1.526e-5 to +1.514e-5	ingredient of IR gain
			-1.520e-5 to +1.514e-5	default : 0
gir	unsigned	GIR[15:0]	$gir = GIR \times 2^{-14}$	IR Gain
gir	urisigned	GIN[15.0]	0 to 4	default : 1.0
oir	cianod	OIR[11:0]	oir = OIR	IR Offset
Oir	oir signed	OIK[11.0]	-2048 to +2047	default : 0

These registers should be written during *MODE* = "0"

10.8. Temperature Calculation(Temp. Calc.)

The temperature calculation result (TO) is obtained from IR' and TS'. IR' and TS' are the results of the correction circuit (10.7).

The flow of the calculation is shown below.

$$F(TS') = fc4 \times TS'^4 + fc3 \times TS'^3 + fc2 \times TS'^2 + fc1 \times TS' + fc0$$

 $G(TS') = gc4 \times TS'^4 + gc3 \times TS'^3 + gc2 \times TS'^2 + gc1 \times TS' + gc0$
 $IM(IR') = (IR' - F(TS')) \times G(TS')$
 $(uf6.10) TO = xc4 \times IM^4 + xc3 \times IM^3 + xc2 \times IM^2 + xc1 \times IM + xc0$

Table 10.5. Calculation coefficient

coefficient	Туре	Register	Value
fc4,gc4,xc4 fc3,gc3,xc3	signed	FC4[15:0], FC4EX[7:0] : XC3[15:0], XC3EX[7:0]	fc4 = $FC4 \times 2^{-(15+FC4EX)}$, fc3 = $FC3 \times 2^{-(15+FC3EX)}$
fc2,gc2,xc2	signed	FC2[15:0], FC2EX[5:0] : XC2[15:0], XC2EX[5:0]	fc2 = FC2×2-(15+FC2EX)
fc1,gc1,xc1	signed	FC1[15:0], FC1EX[4:0] : XC1[15:0], XC1EX[4:0]	fc1 = FC1×2 ^{-(14+FC1EX)}
fc0	signed	FC0[15:0]	fc0 = <i>FC0</i>
gc0	signed	GC0[15:0]]	$gc0 = GC0 \times 2^{-14}$
xc0	unsigned	XC0[15:0]	$xc0 = XC0 \times 2^{-10}$

These registers should be written during MODE = "0"

The occurrence of overflow during a calculation is stored in the *OVF* of the ST register and TO= "0xFFFF".

Setting *CALC* = "1" enables Temperature calculation and setting *CALC* = "0" temperature calculation is bypassed. When *CALC* = "0", IR(setting *THSEL* = "0") or TS(setting *THSEL* = "H") is stored in TO.

10.9. Threshold Jugement

0x7FFF).

Compare Temperature calculation result(TO) with the threshold levels.

The signal to be compared with the threshold is selected from differential of TOLPF and Stream Buffer data, TO or TOLPF.

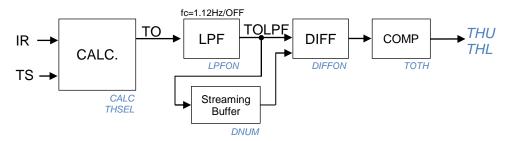


Figure 10.3. Threshold Judgment

Threshold Judgement makes two judgment. TO is changed from below *TOTH* to equal to or above *TOTH*, *THU* turns to "1". TO is changed from above *TOTH* to equal to or below *TOTH*, *THL* turns to "1". The threshold is set by the *TOTH* register.

By setting *LPFON*="1", LPF is applied to the calculate result. When *DIFFON*="1", the signal to be compared with the threshold is the difference between TOLPF and Streaming buffer data. The data of streaming buffer is selected by *DNUM*.

DIFFON="0": Threshold judgment is not performed for the first data after the MODE="1".

DIFFON="1": Threshold judgment is not performed for the number of times set by *DNUM* register.

CALC	THSEL	CALC output	Type	Data	Data(overflow)
0	0	IR[15:0]	signed	0x8001 - 0x7FFE	0x7FFF
0	1	TS[15:0]	signed	0x8001 - 0x7FFE	0x7FFF
1	Х	TO[15:0]	unsigned	0x0001 - 0xFFFE	0xFFFF

When Temperature calculation is disable (*CALC*="0"), IR is stored in *TOUT* if *THSEL*="0", and TS is stored in *TOUT* if *THSEL*="1". When *CALC* is set to "0", *LPFON* should be set to "0". The threshold judgment circuit will not make a judgment when TO=0x0000, 0xFFFF(*CALC*="0", 0x8000,

10.10. Streaming Buffer

AK9757W has a streaming buffer that can store10 samples of TO.

Write "1" to *BUFON* to start storing measurement data to the Streaming Buffer.

The streaming buffer update is stopped under the following conditions, and the data is transferred to the *SB0* to *SB9* registers.

- When BUFON="0" is set.
- If an interrupt occurs when the ITHU,ITHL, or IBFULL register is set to "1".
 BUFON will be automatically set to "0".

To re-start the streaming buffer, set BUFON="1".

Stream Buffer data can be read out from *SB0* to *SB9* Registers. The latest data is stored in the *SB0* register.

BUFON register can be rewritten when either MODE = "0" or "1".

Streaming Buffer is reset when BUFON="1" and the first data is written. The value at reset is 0x8000 when CALON = "0", and 0x0000 when CALON = "1".

10.11. Interrupt Function

INTN output can be used as an interrupt control signal. INTN is an open drain output. INTN outputs the interrupt result ("L") by setting the interrupt setting register(address:23H).

Table 10.6. Interrupt source setting

Register	Address	Data	Description
CNTL4	23H	IOVF	Interrupt is asserted when overflow is occurred in calculation.
		ITHU	Interrupt is asserted when TO is changed from below <i>TOTH</i> to equal or above <i>TOTH</i> .
		ITHL	Interrupt is asserted when TO is changed from above <i>TOTH</i> to equal or below <i>TOTH</i> .
		IBFULL	Interrupt is asserted when streaming buffer is full.
		IDRDY	Interrupt is asserted when a measurement is finished and the AK9757W is ready to read out.

These registers should be written during MODE = "0"

When the calculate is completed, the data registers and status registers are updated and can be read out. At this time, if the interrupt setting is enabled, INTN goes to "L"

The INTN returns to "H", after reading out TOUTL,IRL,TSL or SB0L registers.

When ANG ="1", INTN will be automatically "L" even if there are no accesses to these registers until the next data update timing.

10.12. Measurement Data Read

Measurement data of IR sensors and Temp. Sensor, FOV Temperature calculation data and status data are stored in the following registers.

ST2 is a dummy register for data protect release.

Table 10.7. Measurement Data Registers

rable 10.7. Wedsarement Bata Registers					
Register	Address	Data			
ST	04H	OVF, THU, THL, BFULL, DRDY			
TOUTL	05H	TOUT[7:0]			
TOUTH	06H	TOUT[15:8]			
TSL	07H	TS[7:0]			
TSH	08H	TS[15:8]			
IRL	09H	IR[7:0]			
IRH	0AH	IR[15:8]			
ST2	0BH	-			

Table 10.8. Streaming Buffer Registers

rable refer extearning Barrer registere				
Register	Address	Data		
SB0L	0CH	SB0[7:0]		
SB0H	0DH	SB0[15:8]		
SB1L	0EH	SB1[7:0]		
SB1H	0FH	SB1[15:8]		
SB9L	1EH	SB9[7:0]		
SB9H	1FH	SB9[15:8]		

1.ST Register read out

Table 10.9. ST register

Register	Address	Data	Description
ST	04H	OVF	Indicates Overflow status. When an overflow occurs during a calculation, this bit turns to "1".
		THU	Indicate whether TO exceeds the preset threshold or not. When the TO is changed from below <i>TOTH</i> to equal to or above <i>TOTH</i> , this bit turns to "1".
		THL	Indicate whether TO below the preset threshold or not. When the TO is changed from above <i>TOTH</i> to equal to or a below <i>TOTH</i> , this bit turns to "1".
		BFULL	Indicate Streaming buffer status. When streaming buffer is full, this bit turns to "1".
		DRDY	Indicates Data Ready status. When the latest data is stored, this bit turns to "1".

The status register is judged and updated at the end of the calculation.

The value of these bits are protected and not updated during data read. Data protection is released after reading the *ST2* register or when NACK is returned from the master IC after reading any of the *TOUTH*, *TSH*, *IRH* or *SB0H* registers.

Table 10.10. ST2 register

Re	gister	Address	Data	Description
ST	2	0BH	-	Register for data protection release

2. Measurement Data and Temperature calculation result read out.

Table 10.11 Measurement Data

Register	Address	Data	Description
TOUTL	05H	TOUT[7:0]	Indicate Temperature calculation result. When
TOUTH	06H	TOUT[15:8]	TOUTLPF="1",read the LPF output. Upper 6bit :integer ,Lower 10bit : decimal
TSL	07H	TS[7:0]	Measurement data of integrated Temperature Sensor. 16-bit
TSH	08H	TS[15:8]	data is stored in 2's complement format.
IRL	09H	IR[7:0]	Measurement data of IR Sensor. 16-bit data is stored in 2's
IRH	0AH	IR[15:8]	complement format.

These registers are updated at the end of the calculation.

These registers are protected and not updated during data read. Data protection is released after reading the *ST2* register or when NACK is returned from the master IC after reading any of the *TOUTH*, *TSH,IRH* or *SB0H*.

The value of TO is from 0x0001 to 0xFFFE(9.765e-4 to 63.999023 $^{\circ}$ C). When an overflow occurs during the calculation, the value will be 0xFFFF.

The value of IR and TS is from 0x8001 to 0x7FFE.

10.13. Signal update timing

The ADC operates at the ODR cycle and the internal calculate circuit (CALC) operates when the ADC operation is completed. When the calculate is completed, the data registers and status registers are updated and can be read out. At this time, if the interrupt setting is enabled, INTN goes to "L"

The INTN returns to "H", after reading out *TOUTL*, *IRL*, *TSL* or *SB0L* registers. When *ANG* ="1", INTN will be automatically "L" even if there are no accesses to these registers until the next data update timing.

Data registers(address: 05H to 0AH) are protected and not updated during data read. Data protection is released after reading the *ST2* register or when NACK is returned from the master IC after reading any of the *TOUTH*, *TSH*, *IRH* or *SB0H* registers.

The Data protection of *ST* register is also cleared at the same time.

(Case1) Timing chart in byte read mode

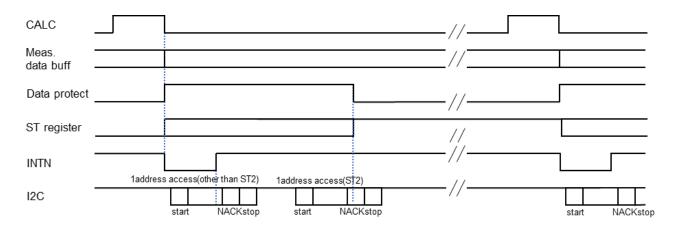


Figure 10.4. case1

(Case2) Timing chart in sequential read

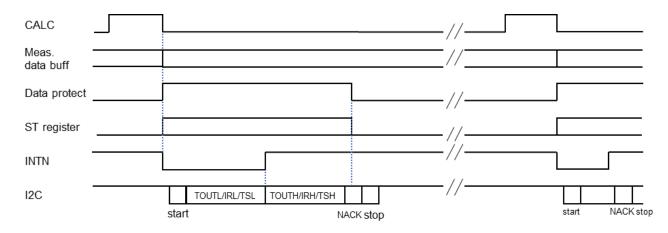


Figure 10.5. case2

(Case3) Timing chart when the read is skipped. (ANG="1")

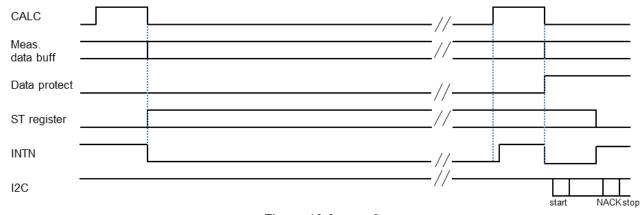


Figure 10.6. case3

11. Sirial Interface

The AK9757W supports I^2C standard mode (max. 100kHz) and fast mode (max. 400kHz). The AK9757W operates as a slave device.

11.1. Data Transfer

Access to the AK9757W through I²C bus after POR.

The master device sends Start condition followed by Slave Address and R/W bit. Then Read/Write operation is executed. Read/Write operation is finished by Stop condition which is generated by the master device.

11.1.1. Changing state of SDA line

The SDA line state should be changed only while the SCL line is "L". The SDA line state must be constant while the SCL line is "H".

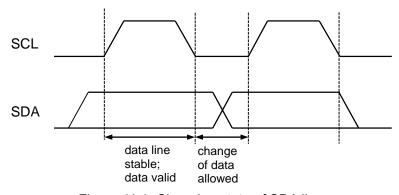


Figure 11.1. Changing state of SDA line

11.1.2. Start/Stop Conditions

All transactions begin with Start condition and finished by Stop condition.

Start condition is generated when the SDA line state is changed from "H" to "L" while the SCL line is "H". Stop condition is generated when the SDA line state is changed from "L" to "H" while the SCL line is "H".

Start/Stop condition are generated by the master device.

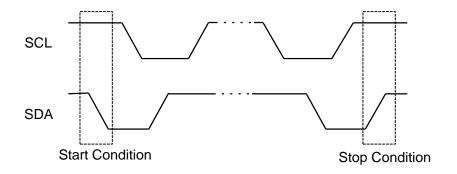


Figure 11.2. Start/Stop Conditions

11.1.3. Acknowledge

The transmitter releases the SDA line (SDA line state to "H") after sending one byte of data. The receiver pulls the SDA line to "L" during the ninth clock pulse is "H". This procedure is called "Acknowledge". The Acknowledge signal indicates that every byte is successfully sent and received. The AK9757W sends Acknowledge after receiving Start condition and the first one byte (Slave Address and R/W bit).

In Write operation, the AK9757W sends Acknowledge after receiving each byte, as the receiver. If the master device sends Stop condition, Write operation is finished.

In Read operation, the AK9757W releases the SDA line after sending each byte and waits for Acknowledge from the master device. After receiving each Acknowledge, the AK9757W sends data. If the master device sends Stop condition, Read operation is finished.

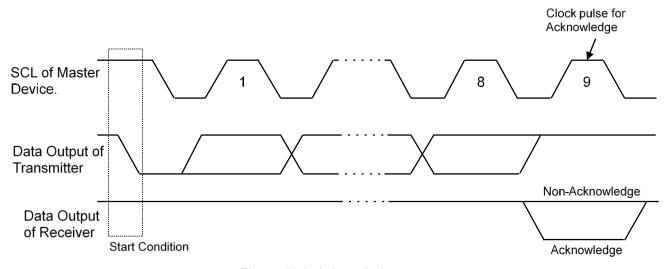


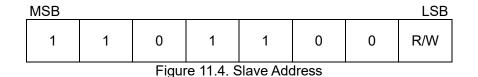
Figure 11.3. Acknowledge

11.1.4. Slave Address

The Slave Address of the AK9757W is 0x6C.

When the master device sends the first one byte (Slave Address and R/W bit) following to Start condition, the device which is specified by the Slave Address on the bus is selected. The device which is specified by the Slave Address sends Acknowledge and then executes command.

The R/W bit is set to "0", Write command is executed. The R/W bit is set to "1", Read command is executed.



11.1.5. WRITE Command

When R/W bit is set to "0", the AK9757W executes Write operation. The master device sends the first one byte (Slave Address and R/W bit) following to Start condition and the AK9757W sends Acknowledge. Then the master device sends address of control register in the second byte. The address consists of 8-bit and MSB-first configuration. After receiving the second byte, the AK9757W sends Acknowledge.

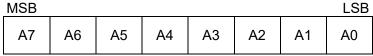


Figure 11.5. Register Address

The master device specifies control data in the third byte. The control data consists of 8-bit and MSB-first configuration. The AK9757W sends Acknowledge after receiving the control data and increments the internal address counter automatically. When the master device sends Stop condition, data transfer is finished.

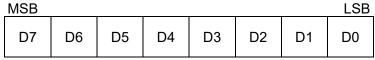
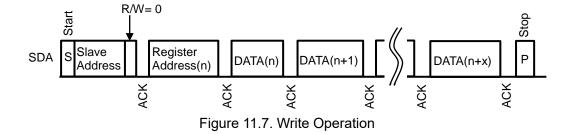


Figure 11.6. Control data

Two or more bytes of data can be written successively.

After receiving the third byte (control data), the AK9757W sends Acknowledge and increments the internal address counter automatically. When receiving the next data, the AK9757W writes data in the next address and increments the internal address counter. If the master device sends Stop condition, the AK9757W finishes Write operation.

For the automatic address increment, please refer Register map (Table 12.2)



11.1.6. READ Command

When the R/W bit is set to "1", the AK9757W executes Read operation.

In Read operation, the AK9757W receives Start condition and the first one byte (Slave address + R/W bit) and sends Acknowledge. Then the AK9757W sends data in the specified address. When the master device sends Stop condition, data transfer is finished.

The AK9757W can read out two or more byte successively. After the AK9757W sends data in the specified address, the master device sends Acknowledge. And the AK9757W sends the data in the next address and increments internal address counter. When the master device sends Stop condition, data transfer is finished.

For the automatic address increment, please refer register map (Table 12.2).

The AK9757W supports Current address read and Random read.

(1) Current Address Read

The AK9757W has the internal address counter. In Read operation, the AK9757W reads out the data which is specified by this counter.

The internal address counter retains the next address which is accessed lastly. For example, if the address which was accessed lastly is "n", the data in address "n+1" is read out by the current address Read operation.

After receiving the first one byte (slave address +R/W bit) following to Start condition, the AK9757W sends Acknowledge. The AK9757W sends 8-bit data specified by internal address counter at the next clock and increments the internal address counter by one. The AK9757W releases the SDA line after sending 8-bit data and waits for Acknowledge from the master device. After receiving Acknowledge, the AK9757W sends data in the next address and increments the internal address counter. If the master device sends Stop condition, Read operation is finished.

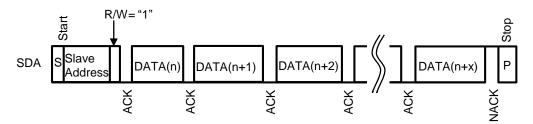


Figure 11.8. Current Address Read

(2) Random Read

Data in an arbitrary address can be read out.

Before sending Slave address and Read command (R/W = "1"), the master device should execute Write command to specify an address start to read out.

After receiving slave address and Write command (R/W = "0") following to Start condition, the AK9757W sends Acknowledge. Second, the master device sends address to read out, and the AK9757W sends Acknowledge. Third, the master device sends Start condition and slave address of Read command (R/W = "1"). Then the AK9757W sends Acknowledge. Next, the AK9757W sends the data in the specified address and increments internal address counter. When the master device sends Acknowledge, the AK9757W sends 8-bit data in the next address and increments the address counter. The master device sends Stop condition, Read operation is finished.

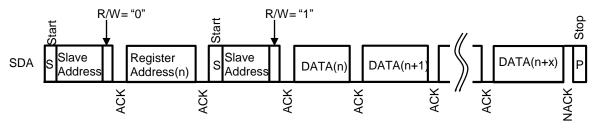


Figure 11.9. Random Read

12. Register Definitions

12.1. Register Map

Table 12.1 Register Map

Address Name			1	ı	14510 12.11	- <u> </u>				
O1H	Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
O2H								0	0	
0.3H										
O4H										
O5H			0				_			
O6H			1	1	1			THL	BFULL	DRDY
O7H										
O8H		TOUTH								
O9H		TS								
OAH	H80	TS				TS[´	15:8]			
OBH	09H	IR				IR[7:0]			
OCH		IR				IR[1	5:8]			
ODH SBUF0 SB0[15:8] OEH SBUF1 SB1[7:0] OFH SBUF1 SB1[7:0] 10H SBUF2 SB2[7:0] 11H SBUF2 SB2[15:8] 12H SBUF3 SB3[7:0] 13H SBUF3 SB3[15:8] 14H SBUF4 SB4[7:0] 15H SBUF4 SB4[7:0] 15H SBUF4 SB4[15:8] 16H SBUF5 SB5[7:0] 17H SBUF5 SB5[7:0] 18H SBUF6 SB6[7:0] 19H SBUF6 SB6[7:0] 19H SBUF6 SB7[7:0] 1BH SBUF7 SB7[15:8] 1CH SBUF8 SB8[7:0] 1DH SBUF8 SB8[7:0] 1DH SBUF8 SB9[7:0] 1FH SBUF9 SB9[7:0] 1FH SBUF9 SB9[7:0] 1FH SBUF9 SB9[7:0] 20H CNTL1 1 <	0BH	ST2	1	1	1	1	1	1	1	1
OEH SBUF1 SB1[7:0] OFH SBUF1 SB1[15:8] 10H SBUF2 SB2[7:0] 11H SBUF2 SB2[15:8] 12H SBUF3 SB3[7:0] 13H SBUF3 SB3[15:8] 14H SBUF4 SB4[7:0] 15H SBUF4 SB4[15:8] 16H SBUF5 SB5[7:0] 17H SBUF5 SB5[7:0] 18H SBUF6 SB6[7:0] 19H SBUF6 SB6[7:0] 19H SBUF7 SB7[7:0] 1BH SBUF7 SB7[15:8] 1CH SBUF8 SB8[7:0] 1DH SBUF8 SB8[7:0] 1DH SBUF8 SB9[7:0] 1FH SBUF9 SB9[7:0] 2H CNTL1 1	0CH	SBUF0				SB0	[7:0]			
OFH SBUF1 SB1[15:8] 10H SBUF2 SB2[7:0] 11H SBUF2 SB2[15:8] 12H SBUF3 SB3[7:0] 13H SBUF3 SB3[15:8] 14H SBUF4 SB4[7:0] 15H SBUF4 SB4[15:8] 16H SBUF5 SB5[7:0] 17H SBUF5 SB5[15:8] 18H SBUF6 SB6[15:8] 18H SBUF6 SB6[15:8] 1AH SBUF7 SB7[7:0] 1BH SBUF7 SB7[15:8] 1CH SBUF8 SB8[7:0] 1DH SBUF8 SB8[7:0] 1EH SBUF9 SB9[7:0] 1FH SBUF9 SB9[15:8] 20H CNTL1 1	0DH	SBUF0				SB0[[15:8]			
10H	0EH	SBUF1				SB1	[7:0]			
SBUF2 SBUF3 SB3[7:0] 13H	0FH	SBUF1								
12H SBUF3 SB3[7:0]	10H	SBUF2		SB2[7:0]						
13H	11H	SBUF2								
14H SBUF4 SB4[7:0] 15H SBUF4 SB4[15:8] 16H SBUF5 SB5[7:0] 17H SBUF5 SB5[15:8] 18H SBUF6 SB6[7:0] 19H SBUF6 SB6[15:8] 1AH SBUF7 SB7[7:0] 1BH SBUF7 SB7[15:8] 1CH SBUF8 SB8[7:0] 1DH SBUF8 SB9[7:0] 1FH SBUF9 SB9[7:0] 1FH SBUF9 SB9[15:8] 20H CNTL1 1	12H	SBUF3				SB3	[7:0]			
15H SBUF4 SB4[15:8] SB5[7:0] SB5[7:0] SB5[7:0] SB5[7:0] SB5[7:0] SB5[7:0] SB6[7:0] SB6[7:0] SB6[7:0] SB6[7:0] SB7[7:0] SB9[7:0] SB9[7	13H	SBUF3				SB3[15:8]			
16H	14H	SBUF4				SB4	[7:0]			
17H	15H	SBUF4				SB4[[15:8]			
18H	16H	SBUF5				SB5	[7:0]			
19H	17H	SBUF5				SB5[[15:8]			
1AH SBUF7 SB7[7:0] 1BH SBUF7 SB7[15:8] 1CH SBUF8 SB8[7:0] 1DH SBUF8 SB8[15:8] 1EH SBUF9 SB9[7:0] 1FH SBUF9 SB9[15:8] 20H CNTL1 1 1 1 1 1 SRST 21H CNTL2 1 1 1 1 1 1 BUFON 22H CNTL3 IROFF GAIN[2:0] CALC dummy ODR[1:0] 23H CNTL4 ANG dummy[1:0] IOVF ITHU ITHL IBFULL IDRDY 24H CNTL5 LPFON TOUTLPF THSEL DIFFON DNUM[3:0] 25H CNTL6 TOTH[15:8] TOTH[15:8] AVN[5:0]	18H	SBUF6				SB6	[7:0]			
1BH SBUF7 SB7[15:8] SB8[7:0] SBUF8 SB8[7:0] SB8[15:8] SB8[15:8] SB9[7:0] SB9[7:0] SB9[7:0] SB9[7:0] SB9[15:8]	19H	SBUF6				SB6[[15:8]			
1CH	1AH	SBUF7				SB7	[7:0]			
1DH	1BH	SBUF7				SB7[[15:8]			
1EH SBUF9 SB9[7:0] 1FH SBUF9 SB9[15:8] 20H CNTL1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 <t< td=""><td>1CH</td><td>SBUF8</td><td></td><td></td><td></td><td>SB8</td><td>[7:0]</td><td></td><td></td><td></td></t<>	1CH	SBUF8				SB8	[7:0]			
1FH SBUF9 SB9[15:8] 20H CNTL1 1	1DH	SBUF8				SB8[[15:8]			
20H CNTL1 1 </td <td>1EH</td> <td>SBUF9</td> <td></td> <td></td> <td></td> <td>SB9</td> <td>[7:0]</td> <td></td> <td></td> <td></td>	1EH	SBUF9				SB9	[7:0]			
21H CNTL2 1 1 1 1 1 1 1 1 BUFON 22H CNTL3 IROFF GAIN[2:0] CALC dummy ODR[1:0] 23H CNTL4 ANG dummy[1:0] IOVF ITHU ITHL IBFULL IDRDY 24H CNTL5 LPFON TOTLPF THSEL DIFFON DNUM[3:0] 25H CNTL6 TOTH[7:0] 26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	1FH	SBUF9				SB9[[15:8]			
22H CNTL3 IROFF GAIN[2:0] CALC dummy ODR[1:0] 23H CNTL4 ANG dummy[1:0] IOVF ITHU ITHL IBFULL IDRDY 24H CNTL5 LPFON TOUTLPF THSEL DIFFON DNUM[3:0] 25H CNTL6 TOTH[7:0] 26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	20H	CNTL1	1	1	1	1	1	1	1	SRST
23H CNTL4 ANG dummy[1:0] IOVF ITHU ITHL IBFULL IDRDY 24H CNTL5 LPFON TOUTLPF THSEL DIFFON DNUM[3:0] 25H CNTL6 TOTH[7:0] 26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	21H	CNTL2	1	1	1	1	1	1	1	BUFON
23H CNTL4 ANG dummy[1:0] IOVF ITHU ITHL IBFULL IDRDY 24H CNTL5 LPFON TOUTLPF THSEL DIFFON DNUM[3:0] 25H CNTL6 TOTH[7:0] 26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	22H	CNTL3	IROFF	IROFF GAIN[2:0] CALC dummy ODR[1:0]						
25H CNTL6 TOTH[7:0] 26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	23H		ANG	dumm	ny[1:0]	IOVF	ITHU		IBFULL	IDRDY
26H CNTL7 TOTH[15:8] 27H CNTL8 1 1 AVN[5:0]	24H	CNTL5	LPFON	TOUTLPF	THSEL	DIFFON		DNU	M[3:0]	
27H CNTL8 1 1 AVN[5:0]	25H	CNTL6				TOTI	H[7:0]		-	
· ·	26H	CNTL7				TOTH	I[15:8]			
28H CNTL9 1 1 1 IRINV Reserved MODE	27H	CNTL8	1 1 AVN[5:0]							
	28H	CNTL9	1	1	1	IRINV		Reserved		MODE

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	
29H	FCOEF4		FC4[7:0]							
2AH	FCOEF4				FC4[15:8]				
2BH	FCOEF4EX				FC4E	X[7:0]				
2CH	FCOEF3				FC3	[7:0]				
2DH	FCOEF3				FC3[15:8]				
2EH	FCOEF3EX				FC3E	X[7:0]				
2FH	FCOEF2				FC2	[7:0]				
30H	FCOEF2				FC2[
31H	FCOEF2EX	1	1			FC2E	X[5:0]			
32H	FCOEF1				FC1	[7:0]				
33H	FCOEF1				FC1[15:8]				
34H	FCOEF1EX	1	1	1			FC1EX[4:0]			
35H	FCOEF0				FC0	[7:0]				
36H	FCOEF0				FC0[15:8]				
37H	GCOEF4				GC4	·[7:0]				
38H	GCOEF4				GC4	[15:8]				
39H	GCOEF4EX				GC4E	X[7:0]				
3AH	GCOEF3				GC3	[7:0]				
3BH	GCOEF3				GC3	[15:8]				
3CH	GCOEF3EX				GC3E	X[7:0]				
3DH	GCOEF2				GC2	[7:0]				
3EH	GCOEF2				GC2	[15:8]				
3FH	GCOEF2EX	1	1			GC2E	X[5:0]			
40H	GCOEF1				GC1	[7:0]				
41H	GCOEF1				GC1	[15:8]				
42H	GCOEF1EX	1	1	1			GC1EX[4:0]			
43H	GCOEF0				GC0	[7:0]				
44H	GCOEF0				GC0	[15:8]				
45H	XCOEF4					[7:0]				
46H	XCOEF4				XC4[[15:8]				
47H	XCOEF4EX					X[7:0]				
48H	XCOEF3				XC3	[7:0]				
49H	XCOEF3					[15:8]				
4AH	XCOEF3EX			XC3EX[7:0]						
4BH	XCOEF2			XC2[7:0]						
4CH	XCOEF2			XC2[15:8]						
4DH	XCOEF2EX	1	1	XC2EX[5:0]						
4EH	XCOEF1			XC1[7:0]						
4FH	XCOEF1			XC1[15:8]						
50H	XCOEF1EX	1	1	-1			XC1EX[4:0]			
51H	XCOEF0			XC0[7:0]						
52H	XCOEF0				XC0[[15:8]				

Address	Name	D7	D6	D5	D4	D4 D3 D2 D1 D0					
53H	reserved	1	1 1 1 Reserved								
54H	GIR				GIR	[7:0]					
55H	GIR		GIR[15:8]								
56H	OIR		OIR[7:0]								
57H	OIR	0	0	0	0		OIR[11:8]			
58H	GTS		GTS[7:0]								
59H	OTS				OTS	[7:0]					
5AH	OTS	0	0			OTS	[13:8]				
5BH	GIT				GIT	[7:0]					
5CH	reserved				Rese	erved					
5DH	reserved	Reserved									
5EH	reserved		Reserved								
5FH	reserved		Reserved								

Table 12.2 Address Increment

Address	Name	Read/ Write	Address Increment	Remark
00H	WIA1	R	•	
01H	WIA2	R		
02H	INFO1	R		
03H	INFO2	R		
04H	ST	R	₹ !	
05H	TOUTL	R		
06H	TOUTH	R	1 1	
07H	TS	R		
08H	TS	R	!	
09H	IR	R		
0AH	IR	R		
0BH	ST2	R	¥i	Returns to address 04H after reading address 0BH
0CH	SBUF0	R	↑ < !	
0DH	SBUF0	R		
0EH	SBUF1	R		
0FH	SBUF1	R	i i	
10H	SBUF2	R	į	
11H	SBUF2	R		
		•	. :	
			<u> </u>	·
1BH	SBUF7	R		
1CH	SBUF8	R	<u> </u>	
1DH	SBUF8	R		
1EH	SBUF9	R		
1FH	SBUF9	R	V!	Returns to address 0CH after reading address 1FH
20H	CNTL1	R/W	† <	
21H	CNTL2	R/W	<u> </u>	
22H	CNTL3	R/W		
23H	CNTL4	R/W	 	
24H	CNTL5	R/W	<u> </u>	
25H	CNTL6	R/W		
26H	CNTL7	R/W		
27H	CNTL8	R/W	l l i -	Returns to address 20H after reading address 28H
28H	CNTL9	R/W	V	Returns to address 20H after reading address 20H
29H	FCOEF4	R/W	↑ < !	
2AH	FCOEF4	R/W	 	
2BH	FCOEF4EX	R/W	 	
2CH	FCOEF3	R/W	 	
2DH	FCOEF3	R/W	 	
2EH	FCOEF3EX	R/W	 	
•				
5BH	GIT	R/W	 	
5CH	reserved	R	 	
5DH	reserved	R	 	
5EH	reserved	R	 	
5FH	reserved	R	 	Returns to address 29H after reading address 5FH
<u> </u>	10001100	1.		<u> </u>

12.2. Function Descriptions

12.2.1. WIA1: Company Code (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	WIA1	0	1	0	0	1	0	0	0

One Byte fixed code as Company code of AKM.

12.2.2. WIA2: Device ID (Read Only Register)

Addres	Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	WIA2	0	0	0	1	0	1	1	1

One Byte fixed code as the AK9757 device ID.

12.2.3. INFO1: Information1 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	INFO1	0	0	0	0	0	0	0	0

INFO1[7:0]: Information for AKM use only.

12.2.4. INFO2: Information2 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	INFO2	0	0	0	0	0	0	0	0

INFO2[7:0]: Information for AKM use only.

12.2.5. ST: Status (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	ST	1	1	1	OVF	THU	THL	BFULL	DRDY
Reset		1	1	1	0	0	0	0	0

Bit	Field	Description
7:5	N.A.	
4	OVF	Indicates Overflow status. "0": Normal State (default)
		"1" : Overflow occurred during a calculation.
3	THU	Indicate whether TO exceeds the preset threshold or not.
		"0" : Normal State (default)
		"1" : TO is changed from below TOTH to equal to or above TOTH.
2	THL	Indicate whether TO below the preset threshold or not.
		"0" : Normal State (default)
		"1" : TO is changed from above TOTH to equal to or below TOTH.
1	BFULL	Indicates Streaming buffer is full.
		"0" : Normal State (default)
		"1" : Streaming buffer is full.
0	DRDY	Indicates Data Ready status.
		"0" : Normal State (default)
		"1" : Data Ready

The value of these bits are protected and not updated during data read. Data protection is released after reading the ST2 register or when NACK is returned from the master IC after reading any of the TOUTH, TSH, IRH or SB0H registers.

12.2.6. TOUT, TS, IR: data register (Read Only Register)

12.2.7. Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	TOUT		TOUT[7;0]						
06H	TOUT[15:8]								
Reset	0000H								

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
07H	TS		TS[7:0]								
H80			TS[15:8]								
09H	IR		IR[7:0]								
0AH			IR[15:8]								
Res	et		8000H								

Name	Description
TOUT	Temperature calculation result data register
	Unsigned 16bit Upper 6bit :integer ,Lower 10bit : decimal
	When CALC="0", IR(THSEL="0") or TS(THSEL="1")
TS	Built-in Temperature sensor data register
	Signed 16bit
IR	IR sensor data register
	Signed 16bit

12.2.8. ST2: Status2 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	ST2	1	1	1	1	1	1	1	1
Reset		1	1	1	1	1	1	1	1

This register is used to release data protection.

12.2.9. SBUFx: Streaming Buffer data (Read Only Register)

			Banor data	(1 1 2 1 2 1 2 1 1	iy rtegieter/							
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0			
0CH	SBUF0		SB0[7;0]									
0DH			SB0[15:8]									
0EH	SBUF1		SB1[7:0]									
0FH					SB1[[15:8]						
10H	SBUF2				SB2	[7:0]						
11H					SB2[[15:8]						
12H	SBUF3				SB3	[7:0]						
13H					SB3[[15:8]						
14H	SBUF4					[7:0]						
15H					SB4[[15:8]						
16H	SBUF5				SB5	[7:0]						
17H					SB5[[15:8]						
18H	SBUF6				SB6	[7:0]						
19H					SB6[[15:8]						
1AH	SBUF7					[7:0]						
1BH					SB7[[15:8]						
1CH	SBUF8				SB8	[7:0]						
1DH					SB8[[15:8]						
1EH	SBUF9				SB9	[7:0]						
1FH			·	·	SB9[[15:8]		·				
Res	set			000	0H (8000H v	when CALC:	="0")					

Name	Description
SBUFx	AK9757W has a streaming buffer that can store10 samples of TO.
	The latest value will be stored in SBUF0.
	When reading out, set BUFON="0".

12.2.10. CNTL1: Soft Reset (Read/Write Register)

					/				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
20H	CNTL1	1	1	1	1	1	1	1	SRST
Reset		1	1	1	1	1	1	1	0

Bit	Field	Description
7:1	N.A.	
0	SRST	Soft Reset "0": Normal State (default) "1": Reset Logic circuit and all registers are reset.
		Logic circuit and all registers are reset. SRST automatically returns to "0" after reset.

12.2.11. CNTL2: Streaming buffer control (Read/Write Register)

			,				/				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
21H	CNTL2	1	1	1	1	1	1	1	BUFON		
Reset		1	1	1	1	1	1	1	0		

Bit	Field	Description
7:1	N.A.	
0	BUFON	Streaming Buffer setting
		"0" : Streaming buffer OFF
		"1" : Streaming buffer ON

When ITHU, ITHL, or IBFULL is set to "1" and an interrupt occurs, BUFON will automatically return to "0"

12.2.12. CNTL3: I/V AMP, Temp. calc., ODR setting (Read/Write Register)

	in the state of th											
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0			
22H	CNTL3	IROFF		GAIN[2:0]			dummy	ODR	R[1:0]			
Reset		0		1H	•	0	0	0	Н			

Bit	Field	Description
7	IROFF	Short-circuit IRINA and IRINC inside the AK9757W.
		"0" : Normal State (default)
		"1" : Shorting IRINÀ and IŔINC
6:4	GAIN	I/V AMP Gain setting
		"000" : x2
		"001": x1 (default)
		"010": x1/2
		"011" : x1/4
		"100" : x1/6
		"101"-"111": Do not use
3	CALC	Enable Temperature calculation
		"0" : Disabled(default)
		"1" : Enabled `
2	dummy	-
1:0	ODR	Output Data Rate(frequency) setting
		"00": 1Hz (default)
		"01": 2Hz `
		"10": 10Hz
		"11" : 50Hz

12.2.13. CNTL4: Interrupt setting (Read/Write Register)

					<u> </u>				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
23H	CNTL4	ANG	dumn	ny[1:0]	IOVF	ITHU	ITHL	IBFULL	IDRDY
Reset 0		0	Н	0	0	0	0	0	

Bit	Field	Description
7	ANG	INTN auto negate setting "0" : Disabled(default) "1" : Enabled
6:5	dummy	-
4	IOVF	Interrupt enable when overflow occurs. "0": Disabled(default) "1": Enabled Interrupt is asserted when overflow is occurred in calculation.
3	ITHU	Interrupt enable when TO exceeds TOTH "0": Disabled (default) "1": Enabled Interrupt is asserted when TO is changed from below TOTH to equal or above TOTH.
2	ITHL	Interrupt enable when TO is below TOTH "0": Disabled (default) "1": Enabled Interrupt is asserted when TO is changed from above TOTH to equal or below TOTH.
1	IBFULL	Interrupt enable when Streaming buffer is full "0": Disabled (default) "1": Enabled Interrupt is asserted when streaming buffer is full.
0	IDRDY	Interrupt enable on Data Ready "0": Disabled (default) "1": Enabled Interrupt is asserted when a measurement is finished and the AK9757W is ready to read out.

12.2.14. CNTL5: Threshold judgment setting (Read/Write Register)

			, ,	<u> </u>		J /			
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
24H	CNTL5	LPFON	TOUTLPF	THSEL	DIFFON		DNU	M[3:0]	
Res	set	0	0	0	0		0	Н	

Bit	Field	Description
7	LPFON	Indicates whether LPF should be applied to the calculation result. "0": Disabled (default) "1": Enabled
6	TOUTLPF	Select the signal to be stored in the TOUT register. "0": Calculation result signal(TO) (default) "1": LPF output (TOLPF)
5	THSEL	Selects the output signal when Temperature calculation is disabled(CALC ="0"). "0": IR (default) "1": TS
4	DIFFON	Setting the input signal for threshold judgment "0": use TOLPF (default) "1": use TOLPF - SBx
3:0	DNUM	Select the Streaming Buffer data(SBx) when DIFFON = "1" "0000": SB0 (latest data) (default) "0010": SB1 "0010": SB2 "0011": SB3 "0100": SB4 "0101": SB5 "0110": SB6 "0111": SB7 "1000": SB8 "1001": SB9 "1010"-"1111": Do not use

12.2.15. CNTL6, CNTL7: Threshold Level setting (Read/Write Register)

Address	Name	D7	D7 D6 D5 D4 D3 D2 D1 D0						
25H	CNTL6		TOTH[7:0]						
26H	CNTL7		TOTH[15:8]						
Res	set				000	00H			

Name	Description
TOTH	Threshold Level
	CALC="0" : unsigned, CALC="1" : signed

12.2.16. CNTL8: ADC average number setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
27H	CNTL8	1	1			AVN	[5:0]		
Res	set	1	1			00)H		·

Bit	Field	Description
7:6	NA	
5:0	AVN	ADC average number setting

ODR[1:0]	0x	00	0x	01	0x	10	0x	11	
	11	Ηz	21	Ηz	10	Hz	50	Hz	
AVN[5:0]	IR path	TS path	IR path	TS path	IR path	TS path	IR path	TS path	
0x00	1	1	1	1	1	1	1	1	
0x01	2	1	2	1	2	1	2	1	
0x02	3	1	3	1	3	1	3	1	
0x03	4	1	4	1	4	1	4	1	
0x04	5	1	5	1	5	1	5	1	
0x05	6	1	6	1	6	1	6	1	
0x06	7	1	7	1	7	1			
0x07	8	1	8	1	8	1			
80x0	9	2	9	2	9	2			
0x09	10	2	10	2	10	2			
:	:	:	:	:	:	:			
0x1E	31	4	31	4	31	4			
0x1F	32	4	32	4	32	4			
0x20	64	8	64	8					
0x21	96	12	96	12					
0x22	128	16	128	16			Do no	ot use	
0x23	160	20	160	20					
0x24	192	24							
0x25	224	28			Do no	ot use			
0x26	256	32			DOTIC	n use			
0x27	288	36	Do not use						
0x28	320	40							
0x29									
:	Do no	ot use							
0x3F									

12.2.17. CNTL9: Mode setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
28H	CNTL9	1	1	1	IRINV		Reserved		MODE
Res	set	1	1	1	0	0	0	0	0

Bit	Field	Description
7:5	NA	
4	IRINV	Invert setting for IR signal after AD conversion. "0": Normal(default) "1": Invert
3:1	Reserved	When writing these registers, you must set these bits to "0"
0	MODE	Operation Mode setting "0" : Stand-By Mode(default) "1" : Continuous Measurement Mode

12.2.18. FCOEF4,FCOEF4EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7									
29H	FCOEF4		FC4[7:0]								
2AH	FCOEF4				FC4[15:8]					
F	Reset				000)0H					
2BH	FCOEF4EX				FC4E	X[7:0]					
F	Reset	00H									

Set the coefficient fc4 of the calculation by the following formula. The type of this coefficient is singed. **fc4** = $FC4 \times 2^{-(15+FC4EX)}$

12.2.19. FCOEF3,FCOEF3EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	DΛ	
Address	ivame	וט	סט	บอ	D4	บง	DZ	וט	D0	
2CH	FCOEF3		FC3[7:0]							
2DH	FCOEF3				FC3[15:8]				
F	Reset				000)0H				
2EH	FCOEF3EX				FC3E	X[7:0]				
F	Reset		00H							

Set the coefficient fc3 of the calculation by the following formula. The type of this coefficient is singed. **fc3** = $FC3 \times 2^{-(15+FC3EX)}$

12.2.20. FCOEF2,FCOEF2EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
2FH	FCOEF2		FC2[7:0]								
30H	FCOEF2				FC2[[15:8]					
F	Reset				000	00H					
31H	FCOEF2EX	1	1			FC2E	X[5:0]				
F	Reset C0H										

Set the coefficient fc2 of the calculation by the following formula. The type of this coefficient is singed. $fc2 = FC2 \times 2^{-(15+FC2EX)}$

12.2.21. FCOEF1,FCOEF1EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
32H	FCOEF1		FC1[7:0]								
33H	FCOEF1		FC1[15:8]								
F	Reset				000	00H					
34H	FCOEF1EX	1	1	1			FC1EX[4:0]				
F	Reset	E0H									

Set the coefficient fc1 of the calculation by the following formula. The type of this coefficient is singed. **fc1** = FC1 \times 2^{-(14+FC1EX)}

12.2.22. FCOEF0,FCOEF0EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D7 D6 D5 D4 D3 D2 D1 D0							
35H	FCOEF0		FC0[7:0]							
36H	FCOEF0				FC0[[15:8]				
R	leset		0000H							

Set the coefficient fc0(**fc0** = FC0). The type of this coefficient is singed.

12.2.23. GCOEF4,GCOEF4EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
37H	GCOEF4		GC4[7:0]								
38H	GCOEF4				GC4	[15:8]					
F	Reset				000)0H					
39H	GCOEF4EX				GC4E	X[7:0]					
Reset 00H											

Set the coefficient gc4 of the calculation by the following formula. The type of this coefficient is singed. $gc4 = GC4 \times 2^{-(15+GC4EX)}$

12.2.24. GCOEF3,GCOEF3EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7								
3AH	GCOEF3		GC3[7:0]							
3BH	GCOEF3				GC3	[15:8]				
F	Reset				000	OOH				
3CH	GCOEF3EX				GC3E	X[7:0]				
F	Reset	00H								

Set the coefficient gc3 of the calculation by the following formula. The type of this coefficient is singed. $gc3 = GC3 \times 2^{-(15+GC3EX)}$

12.2.25. GCOEF2,GCOEF2EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
3DH	GCOEF2		GC2[7:0]								
3EH	GCOEF2				GC2	[15:8]					
F	Reset				000	DOH.					
3FH	GCOEF2EX	1	1			GC2E	X[5:0]				
F	Reset	СОН									

Set the coefficient gc2 of the calculation by the following formula. The type of this coefficient is singed. $gc2 = GC2 \times 2^{-(15+GC2EX)}$

12.2.26. GCOEF1,GCOEF1EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0			
40H	GCOEF1		GC1[7:0]									
41H	GCOEF1		GC1[15:8]									
F	Reset				000)0H						
42H	GCOEF1EX	1	1	1			GC1EX[4:0]					
F	Reset				E0H							

Set the coefficient gc1 of the calculation by the following formula. The type of this coefficient is singed. $gc1 = GC1 \times 2^{-(14+GC1EX)}$

12.2.27. GCOEF0,GCOEF0EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D7 D6 D5 D4 D3 D2 D1 D0								
43H	GCOEF0		GC0[7:0]								
44H	GCOEF0				GC0	[15:8]					
F	Reset		0000H								

Set the coefficient gc0(gc0 = GC0 \times 2⁻¹⁴). The type of this coefficient is singed.

12.2.28. XCOEF4,XCOEF4EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7									
45H	XCOEF4		XC4[7:0]								
46H	XCOEF4				XC4[15:8]					
F	Reset				000)0H					
47H	XCOEF4EX		XC4EX[7:0]								
F	Reset	00H									

Set the coefficient xc4 of the calculation by the following formula. The type of this coefficient is singed. $\mathbf{xc4} = \mathbf{XC4} \times 2^{-(15+\mathbf{XC4EX})}$

12.2.29. XCOEF3,XCOEF3EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0		
48H	XCOEF3		XC3[7:0]								
49H	XCOEF3				XC3	[15:8]					
F	Reset				000	DOH.					
4AH	XCOEF3EX				XC3E	X[7:0]					
F	Reset	00H									

Set the coefficient xc3 of the calculation by the following formula. The type of this coefficient is singed. $\mathbf{xc3} = \mathbf{XC3} \times 2^{-(15+\mathbf{XC3EX})}$

12.2.30. XCOEF2,XCOEF2EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
4BH	XCOEF2		XC2[7:0]						
4CH	XCOEF2		XC2[15:8]						
F	Reset		0000H						
4DH	XCOEF2EX	1	1 1 XC2EX[5:0]						
F	Reset		C0H						

Set the coefficient xc2 of the calculation by the following formula. The type of this coefficient is singed. $xc2 = XC2 \times 2^{-(15+XC2EX)}$

12.2.31. XCOEF1,XCOEF1EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	
4EH	XCOEF1		XC1[7:0]							
4FH	XCOEF1		XC1[15:8]							
F	Reset		0000H							
50H	XCOEF1EX	1	1 1 1 XC1EX[4:0]							
Reset			E0H							

Set the coefficient xc1 of the calculation by the following formula. The type of this coefficient is singed. $xc1 = XC1 \times 2^{-(14+XC1EX)}$

12.2.32. XCOEF0,XCOEF0EX: Calculation coefficient setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
51H	XCOEF0				XC0	[7:0]			
52H	XCOEF0		XC0[15:8]						
F	Reset				000	DOH			

unsigned

Set the coefficient xc0 of the calculation by the following formula. The type of xc0 is unsinged.

 $xc0 = XC0 \times 2^{-10}$

12.2.33. reserved (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
53H	reserved	1	1	1			Reserved		
Re	set	1	1	1	0	0	0	0	0

Bit	Field	Description
7:5	NA	
4:0	Reserved	When writing these registers, you must set these bits to "0"

12.2.34. GIR: IR gain Correction parameter setting (Read/Write Register)

	•	· 9			.9 (. 100.0, 11		• /		
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
54H	GIR		GIR[7:0]						
55H	GIR		GIR[15:8]						
Re	set				400)0H			

Set the correction parameter gir by the following formula. The type of this coefficient is unsinged. $gir = GIR \times 2^{-14}$

12.2.35. OIR: IR offset Correction parameter setting (Read/Write Register)

					<u> </u>				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
56H	OIR				OIR	[7:0]			
57H	OIR	0	0	0	0		OIR[11:8]	
Res	set		0000H						

Set the correction parameter oir(**oir** = OIR). The type of this coefficient is singed.

12.2.36. GTS: TS Gain Correction parameter setting (Read/Write Register)

					<u> </u>				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
58H	GTS		GTS[7:0]						
Res	set				00)H			

Set the correction parameter gts by the following formula. The type of this coefficient is singed.

gts = GTS \times 2⁻¹⁰

12.2.37. OTS: TS offset Correction parameter setting (Read/Write Register)

					<u> </u>				
Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
59H	OTS			OTS[7:0]					
5AH	OTS	0	0			OTS	[13:8]		
Res	set		•	0000H					

Set the correction parameter ots(**ots** = OTS). The type of this coefficient is singed.

12.2.38. GIT: Temperature dependent ingredient of IR gain setting (Read/Write Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
5BH	GIT				GIT	[7:0]			
Res	set		00H						

Set the correction parameter git by the following formula. The type of this coefficient is singed.

git = $GIT \times 2^{-23}$

12.2.39. reserved (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
5CH									
5DH	roconvod				Poor	n rod			
5EH	reserved				Rese	erveu			
5FH									
Re	set	00H							

13. Recommended External Circuits

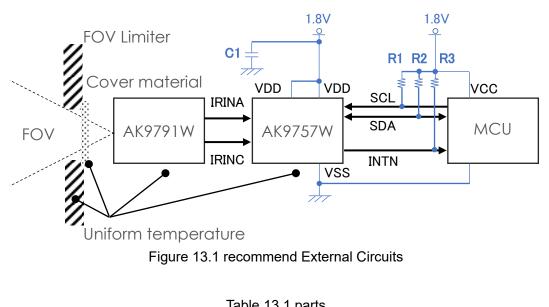


Figure 13.1 recommend External Circuits

Table 13.1 parts

Parts No.	Value	Comment
C1	0.1μF	Ceramic Capacitor
R1	10kΩ	Pull-up Resister
R2	10kΩ	Pull-up Resister
R3	10kΩ	Pull-up Resister

14. Ordering Guide

AK9757W -30 to 85°C wafer

15. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
2023/02	00	First edition	-	-
2023/05/19	01	Correction	30	IC name typo corrected (AK9756→AK9757).
2023/06/22	02	Correction	17	Corrected ITHU description (same notation as p.34).
			14	Coefficient font corrected to bold.
			38,39	Unified table formatting.

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